Effective electrothermal analysis of electronic devices and systems with parameterized macromodeling

Francesco Ferranti, *Member, IEEE,* Alessandro Magnani, Vincenzo d'Alessandro, Salvatore Russo, Niccolò Rinaldi, *Member, IEEE,* Tom Dhaene, *Senior Member, IEEE,* and Massimiliano de Magistris, *Senior Member, IEEE*

***Abstract*—We propose a parameterized macromodeling methodology to effectively and accurately carry out dynamic electrothermal simulations of electronic components and systems, while taking into account the influence of key design parameters on the system behavior. In order to improve the accuracy and to reduce the number of the computationally expensive thermal simulations needed for the macromodel generation, a decomposition of the frequency-domain data samples of the thermal impedance matrix is proposed. The approach is applied to study the impact of layout variations on the dynamic electrothermal behavior of a state-of-the-art 8-finger AlGaN/GaN HEMT grown on a SiC substrate. Simulation results confirm the high accuracy and computational gain obtained by using parameterized macromodels instead of a standard method based on iterative complete numerical analysis.**

***Keywords*—compact thermal modeling, electrothermal simulation, equivalent network, parameterized macromodeling, thermal feedback, thermal impedance, transient analysis.**

I. Introduction

In modern electronic components and systems, thermal effects can heavily affect both reliability and performance if the thermal design is poorly defined. These effects can be related to several factors, such as increase in power density induced by high integration levels, use of insulation schemes based on silicon dioxide, and adoption of advanced materials suffering from poor thermal conductivity (e.g., GaAs and AlGaN). The thermal design can be improved by resorting to accurate electrothermal (ET) simulations, and several analysis methods have been considered [1], [2].

Since it is well established that any heat diffusion problem, once discretized, can be directly interpreted by means of an equivalent electrical network [3], [4], ET simulations can be conveniently pursued by properly defining an electrical equivalent *thermal feedback* (TF) *network*. For affordable system-level ET analyses to be performed within standard circuit simulation tools, it is highly desirable that such TF networks are reduced to minimum complexity for a prescribed accuracy. This goal can be achieved by following classical order-reduction techniques. Discretized thermal equations can be indeed directly reduced in different ways [5], still keeping the integration of the obtained reduced model to the electrical equations level.

An interesting approach is based on the identification of *compact thermal models*, i.e., models describing the heat propagation through the component/system at defined regions of interest by resorting to the *thermal impedance matrix* [6], [7]. Following this approach, the thermal problem is first analyzed with standard 3-D numerical tools, by which data samples of the thermal step response at prescribed input/output ports of the system are computed; then, from such data, a TF network is identified and subsequently used in ET simulations, with great advantage in terms of affordability. However, a number of preliminary CPU/memory demanding 3-D thermal simulations is required (in principle one for each heat source) exploting numerical solvers based, for example, on the finite element method (FEM) [6], [7]. Considering that a typical design process includes activities such as parameters space exploration and variability analysis, both the mesh generation and the whole set of simulations must be repeated for several values of the design parameters (e.g., layout features), which leads to a very significant computational cost.

Parameterized (also called *parametric* or *scalable*) macromodels can be used to speed up design steps without compromising the reliability and accuracy of the results. These models accurately and efficiently represent the system behavior at the input/output ports (e.g., scattering, admittance or impedance representations) parameterized in terms of the design parameters. A limited amount of computationally expensive numerical simulations is needed for their generation. Over the years, different parameterized macromodeling techniques have been proposed [8]–[13] for a large variety of applications, namely, high-speed interconnects, microwave filters, and spiral inductors.

This paper, which extends and completes the study reported in [14], proposes a parameterized macromodeling approach for effective ET simulations of electronic components and systems. In particular, the parameterized thermal modeling introduced in [14] is here improved from the accuracy point of view, and is synthesized into SPICE-like circuits by which full ET simulations are carried out for a relevant case study.

This paper is organized as follows. In Section II, we briefly

F. Ferranti is with the Dept. of Fundamental Electricity and Instrumentation, Vrije Universiteit Brussel, B-1050 Brussels, Belgium (email: francesco.ferranti@vub.ac.be).

A. Magnani, V. d'Alessandro, N. Rinaldi, and M. de Magistris are with the Dept. of Electrical Engineering and Information Technology, University Federico II, 80125 Naples, Italy.

S. Russo is with Meridiana Italia S.r.l., 00187 Rome, Italy.

T. Dhaene is with the Dept. of Information Technology (INTEC), Ghent University-iMinds, Gaston Crommenlaan 8 Bus 201, 9050 Ghent, Belgium.

recall the definition and properties of compact thermal models and thermal impedances. In Section III, the problem of the extraction of a parameterized thermal macromodel is tackled and solved through the method presented in [12]; in particular, a separate identification of the static and dynamic part of thermal impedances is proposed and implemented. In Section IV, the procedure for the macromodel synthesis into SPICE circuits is described. In Section V, the proposed approach is applied to the SPICE-based dynamic ET analysis of a state-of-the-art multi-finger AlGaN/GaN High-Electron Mobility Transistor (HEMT) grown on a SiC substrate, and the results are discussed. Conclusions are then given in Section VI.

II. Compact thermal modeling

Integrating thermal modeling into electrical (circuit) simulation is a major issue in the design workflow of any electronic device and system. A viable approach to perform fully coupled ET simulations is the so-called *compact thermal modeling*, which is based on a procedure articulated into the following steps:

- the thermal problem is described as an "input-output" process, where the heat dissipation takes place in some specific regions (heat sources) and the temperature is to be modeled only in assigned positions, which are relevant from an electrical viewpoint (e.g., at the system terminals);
- after a suitable definition of the regions of interest, a compact, yet accurate, model of the heat propagation can obtained with standard multi-port approaches or alternative numerical-heuristic methods.

A compact thermal model can be graphically represented as in Fig. 1. The *average* temperature rises ΔT_i induced by the dissipation of the spatially dependent power densities $g_i(\mathbf{r})$ (with integral P_{Di}) can be modeled through an equivalent circuit, with ΔT_i corresponding to voltages and P_{Di} to currents. Such correspondence is theoretically sound since there is a formal equivalence between a suitable RC network and (i) any spatial discretization of the linear Fourier conduction equation, and (ii) its solution as an eigenvalue problem [3], [4].

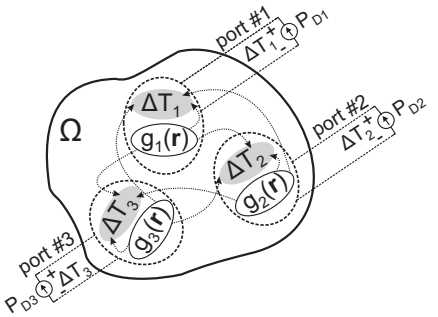

Fig. 1. Schematic representation of the compact thermal model for a problem with 3 heat sources [3], [4].

Let us denote as M_{HS} the number of heat sources, and assume a linear thermal problem. As a consequence, the thermal behavior of the system is completely described by a $M_{HS} \times M_{HS}$ thermal impedance matrix $\mathbf{Z}$, with element $Z_{ij}(t)$ [K/W] defined as the normalized thermal step response, i.e., the temperature rise over ambient of the *i*-th source due to the application of a power step to the *j*-th source, normalized by its amplitude

$$Z_{ij}(t) = \frac{\Delta T_i(t)}{P_{Dj}} = \frac{\Delta T_j(t)}{P_{Di}} \tag{1}$$

$Z_{ii}(t)$ elements are referred to as *self-heating* thermal impedances, while $Z_{ij}(t)$ elements with $i \neq j$ are denoted as *mutual* thermal impedances. It must be remarked that, in spite of the (unfortunate) nomenclature, the mutual impedance must be considered as an indicator of the thermal coupling degree between the heat sources. The steady-state values of the thermal impedances are referred to as thermal resistances.

$\mathbf{Z}$ is usually evaluated with M_{HS} onerous 3-D FEM simulations, in which only one heat source is activated at a time, according to the previous definitions. Regardless of the specific tools used, the accuracy requirements and the corresponding computational cost, this is an "off-line" and "one shot" step in the design workflow.

Once $\mathbf{Z}$ is known, it can be accurately identified with low-order models through various approaches, thereby leading to compact thermal models. In particular, we refer here to standard techinques operating either in the frequency [6] or the time [7], [15] domain.

III. Parameterized macromodeling technique

When the design space is to be explored in terms of some parameters, the procedure for the identification of compact thermal models must be in principle performed for any point in the parameter space. In particular, if the geometrical features of the system are varied, a new mesh generation is required, and the CPU/memory demanding 3-D FEM simulations to evaluate $\mathbf{Z}$ are to be repeated. A drastic reduction in such effort can be achieved by using the so-called *parameterized macromodeling* approach. We discuss here the application of the technique presented in [12], which generates a parameterized macromodel $\mathbf{H}_{model}(s, \mathbf{g})$ to accurately represent a set of multidimensional data samples $\{(s_f, \mathbf{g}_k), \mathbf{H}(s_f, \mathbf{g}_k)\}$, $f = 1, ..., F$, $k = 1, ..., K_{tot}$ which depend on the complex frequency $s = j\omega$ and M design variables $\mathbf{g} = (\mathrm{g}^{(m)})_{m=1}^{M}$, such as layout or substrate features. A parameterized macromodel in a pole-residue form

$$\mathbf{H}_{model}(s, \mathbf{g}) = \mathbf{C}_0(\mathbf{g}) + \sum_{n=1}^{N(\mathbf{g})} \frac{\mathbf{C}_n(\mathbf{g})}{s - p_n(\mathbf{g})} \tag{2}$$

where N is the number of poles, or in a state-space form

$$\mathbf{H}_{model}(s, \mathbf{g}) = \mathbf{C}(\mathbf{g}) \left(s\mathbf{I} - \mathbf{A}(\mathbf{g})\right)^{-1} \mathbf{B}(\mathbf{g}) + \mathbf{D}(\mathbf{g}) \tag{3}$$

is computed. The design space contains all design parameters $\mathbf{g}$ and two design space data grids are used in the modeling process, namely, an *estimation* grid and a *validation* grid. The estimation grid is adopted to build a parameterized macromodel, while the validation grid is employed to verify its accuracy in a set of points of the design space previously not used for the model generation. The method in [12] first identifies a set of rational univariate macromodels $\mathbf{H}_{model}(s, \mathbf{g}_k)$, which are called *root macromodels*, at the estimation design space

points. Then, the estimation design space grid is divided into cells using hyperrectangles (regular grids) or simplices (regular and scattered grids). The validation set points are located at the center of the cells of the estimation grid. Fig. 2 shows a possible 2-D estimation and validation set with rectangular grid cells.

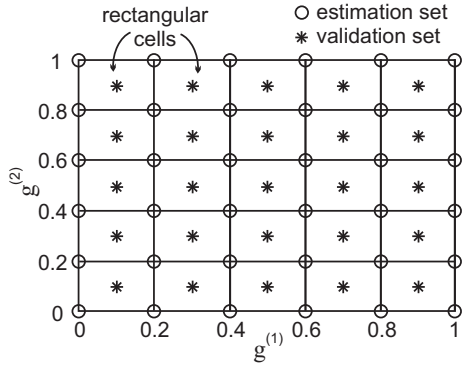

Fig. 2. Estimation and validation set with rectangular grid cells (normalized $\mathrm{g}^{(1)}, \mathrm{g}^{(2)}$ are considered).

Once the estimation design space grid is divided into cells, a local parameterized macromodel is associated to each cell that is a subdomain of the entire design space. We indicate a cell region of the design space as $\Omega_i,\ i = 1, ..., P$ and the corresponding vertices as $\mathbf{g}_k^{\Omega_i},\ k = 1, ..., Q$. We note that each vertex corresponds to a *root macromodel* $\mathbf{H}_{model}(s, \mathbf{g}_k^{\Omega_i})$. For each cell, an optimization procedure is used to find amplitude and frequency scaling coefficients that make each vertex *root macromodel* an accurate approximant of the other cell vertices values (an error function to be minimized regulates the quality of this approximation). For each vertex $\mathbf{H}_{model}(s, \mathbf{g}_k^{\Omega_i})$, a set of amplitude $\alpha_{1,k}(\mathbf{g}_j^{\Omega_i}),\ j = 1, \ldots, Q$ and frequency $\alpha_{2,k}(\mathbf{g}_j^{\Omega_i}),\ j = 1, \ldots, Q$ scaling real coefficients are calculated, using the following optimization step:

$$\min_{\substack{\alpha_{1,k}(\mathbf{g}_j^{\Omega_i}) \\ \alpha_{2,k}(\mathbf{g}_j^{\Omega_i})}} Err(\widetilde{\mathbf{H}}_{model}(s, \mathbf{g}_k^{\Omega_i}), \mathbf{H}_{model}(s, \mathbf{g}_j^{\Omega_i}) \text{ or } \mathbf{H}(s_f, \mathbf{g}_j^{\Omega_i})) \tag{4}$$

with

$$\widetilde{\mathbf{H}}_{model}(s, \mathbf{g}_k^{\Omega_i}) = \alpha_{1,k}(\mathbf{g}_j^{\Omega_i}) \mathbf{H}_{model}(s\alpha_{2,k}(\mathbf{g}_j^{\Omega_i}), \mathbf{g}_k^{\Omega_i}) \tag{5}$$

$$\alpha_{1,k}(\mathbf{g}_j^{\Omega_i}) = \alpha_{2,k}(\mathbf{g}_j^{\Omega_i}) = 1 \text{ if } j = k \tag{6}$$

$$\alpha_{1,k}(\mathbf{g}_j^{\Omega_i}) \geq 0 \tag{7}$$

$$\alpha_{2,k}(\mathbf{g}_j^{\Omega_i}) > 0 \tag{8}$$

The amplitude and frequency scaling coefficients modify the response of a vertex *root macromodel* such that it is able to accurately approximate the behavior of the system under study at the other cell vertices $\mathbf{g}_j^{\Omega_i}$. The reference terms to be approximated in the optimization step can be the *root macromodel* $\mathbf{H}_{model}(s, \mathbf{g}_j^{\Omega_i})$ or the data samples $\mathbf{H}(s_f, \mathbf{g}_j^{\Omega_i})$ at the other vertices $\mathbf{g}_j^{\Omega_i}$. An error function (4) between two frequency responses has to be minimized by this optimization step. If the reference term is $\mathbf{H}_{model}(s, \mathbf{g}_j^{\Omega_i})$, then the number of samples of $s = j\omega$ for which the two frequency responses are compared is not fixed and can be chosen. If the reference term is $\mathbf{H}(s_f, \mathbf{g}_j^{\Omega_i})$, then the number of samples of $s = j\omega$ is fixed since it depends on the available data. This use of amplitude and frequency scaling coefficients allows each vertex *root macromodel* of a specific cell to be able to describe the behavior of the system under study at the other cell vertices $\mathbf{g}_j^{\Omega_i}$. Once all models associated with the design space cells have been generated, the evaluation of the model representation (2)-(3) in a generic point in the design space is straightforward. The design space cell containing this generic point is found and a double interpolation step is performed to evaluate the model at that point [12]. A first interpolation step is applied to the scaling coefficients, which generates scaled *root macromodels*. Finally, an interpolation step at the transfer function level is performed on the scaled *root macromodels*. Further details about this macromodeling technique can be found in [12] and are not repeated here.

In this paper, parameterized macromodels for the thermal behavior of electronic components and systems are investigated. The thermal impedance matrix $\mathbf{Z}$ is modeled as a function of frequency and additional design parameters $\mathbf{g}$. A decomposition of the frequency-domain data samples of $\mathbf{Z}$ is presented to enhance the modeling accuracy and limit the computational cost of the simulations needed for the macromodel generation. Considering the set of thermal impedance matrices at the estimation points $\mathbf{Z}(s_f, \mathbf{g}_k)$, the corresponding DC value $\mathbf{R}(\mathbf{g}_k)$ is extracted and the initial impedance data samples are pre-processed as

$$\widehat{\mathbf{Z}}(s_f, \mathbf{g}_k) = \mathbf{Z}(s_f, \mathbf{g}_k) \circ \mathbf{G}(\mathbf{g}_k) \tag{9}$$

where $\circ$ denotes the Hadamard product [16] (entrywise product of two matrices of the same size) and $\mathbf{G}(\mathbf{g}_k)$ is the Hadamard inverse of $\mathbf{R}(\mathbf{g}_k)$ and therefore each of its entries is

$$G_{ij}(\mathbf{g}_k) = (R_{ij}(\mathbf{g}_k))^{-1} \tag{10}$$

The matrix $\mathbf{R}$ is real, symmetric with all positive elements and positive definite. Two macromodels are generated, $\widehat{\mathbf{Z}}_{model}(s, \mathbf{g})$ and $\mathbf{R}_{model}(\mathbf{g})$ starting from the data samples $\widehat{\mathbf{Z}}(s_f, \mathbf{g}_k)$ and $\mathbf{R}(\mathbf{g}_k)$, respectively. $\mathbf{R}_{model}(\mathbf{g})$ does not depend on frequency and therefore a parameterized macromodel can be built using standard interpolation/approximation models (e.g., radial basis functions, polynomials, splines, etc.). Once both macromodels are generated, the model $\mathbf{Z}_{model}(s, \mathbf{g})$ representing the original thermal impedance data samples can be expressed as

$$\mathbf{Z}_{model}(s, \mathbf{g}) = \widehat{\mathbf{Z}}_{model}(s, \mathbf{g}) \circ \mathbf{R}_{model}(\mathbf{g}) \tag{11}$$

Considering a pole-residue form for $\widehat{\mathbf{Z}}_{model}(s, \mathbf{g})$

$$\widehat{\mathbf{Z}}_{model}(s, \mathbf{g}) = \mathbf{C}_0(\mathbf{g}) + \sum_{n=1}^{N(\mathbf{g})} \frac{\mathbf{C}_n(\mathbf{g})}{s - p_n(\mathbf{g})} \tag{12}$$

then (11) can be written as

$$\mathbf{Z}_{model}(s,\mathbf{g}) = \\ = \mathbf{C}_0(\mathbf{g}) \circ \mathbf{R}_{model}(\mathbf{g}) + \sum_{n=1}^{N(\mathbf{g})} \frac{\mathbf{C}_n(\mathbf{g}) \circ \mathbf{R}_{model}(\mathbf{g})}{s - p_n(\mathbf{g})} \qquad (13)$$

It is worth remarking that this data decomposition is important for two main reasons:

- it allows enhancing the accuracy of the macromodel;
- it allows extracting the DC information of the thermal impedance matrix and modeling it separately. The computational resources needed to evaluate the data samples of the frequency-dependent thermal response $\mathbf{Z}(s_f, \mathbf{g}_k)$ (dynamic thermal simulations) are much more significant than in the case of the computation of only the related DC value $\mathbf{R}(\mathbf{g}_k)$ (steady-state thermal simulations). The sampling in the design space to get dynamic and steady-state thermal response data samples can be decoupled, which helps reduce the overall computational cost to build a parameterized macromodel.

IV. Study workflow and procedure for dynamic electrothermal simulations

The workflow for the extraction of the parameterized macromodel can be described as follows:

- The parameterized macromodel extraction requires to perform numerical simulations of the 3-D structure for a few sets of design parameters. First, the thermal impedance matrices corresponding to the estimation and the validation points are computed through 3-D FEM transient simulation with logarithmically spaced time samples so as to capture the full evolution of the heat conduction.
- The full time-constant spectrum of the thermal impedances is achieved through the *network identification by deconvolution* approach [6], [17], [18]; the time-domain data are thus converted into frequency-domain data.
- The frequency-domain data are identified using the Vector Fitting [19], [20], by which reduced-order root macromodels with around 20 poles are derived for each grid node.
- The parameterized macromodel is then obtained as outlined in Section III. It allows determining the thermal impedance matrix for any point in the design space so as to prevent (i) generating a new mesh and (ii) simulating a new matrix for any layout variation.
- Each thermal impedance matrix corresponding to a point in the design space can be synthesized by resorting to the *thermal equivalent of the Ohm's law*: the temperatures and dissipated powers are represented as voltages and currents, respectively. As a result, a SPICE-like circuit in a netlist form is obtained, which allows describing the power-temperature feedback, and is therefore designated as TF block (TFB). Different topologies can be generated, such as the multi-port Foster scheme [4], [21] and the standard Foster network [7], [22], the latter being employed in this work.

The TFB, besides enabling purely thermal analyses with arbitrary power profiles that would be unviable with pure FEM, can be also used to perform extremely effective ET simulations, as schematically depicted in Fig. 3 [6], [7]:

- The electronic active components are implemented by means of the following procedure: the standard device is replaced by a subcircuit equipped with the conventional electrodes and two additional terminals, namely, an input node fed with the temperature rise above ambient, and an output node providing the dissipated power. The subcircuit is composed by (i) a standard device component as a main element, as well as (ii) resistances, and supplementary linear/nonlinear controlled sources to include specific physical mechanisms and to allow the variation of the temperature-sensitive parameters during the simulation run.
- The electrical macromodels are connected to the TFB in order to account for the power-temperature feedback: the temperature rise provided to each electrical device is determined at any time instant from the powers dissipated by all the active components, i.e., the heat sources in the thermal model.
- As a result, the dynamic ET behavior of the electronic system is represented by a merely electrical network that can be solved by a commercial circuit simulator with little requirement in terms of CPU time and memory storage, as well as reduced possibility of convergence problems.
- It is worth noting that the considered parameterized macromodeling technique is, in its current form, only applicable to structures described by a linear thermal model. As a consequence, nonlinear thermal effects cannot be taken into account. It is in principle possible to provide an *a-posteriori* correction by applying the Kirchhoff transformation [23] to the linear temperatures calculated by the TFB. However, this might lead to inaccurate results if exploited for dynamic simulations [24] or even for steady-state analyses in structures composed of multiple layers with a different temperature dependence of the thermal conductivity [25], [26].

The aforementioned approach is suited to perform fast and effective dynamic ET analyses of electronic systems, circuits, and multicellular / multifinger devices, as described for a case study in the following Section.

V. Case study

HEMTs are unipolar field-effect devices where the current conduction is due to a 2-D electron gas flowing through a low-resistivity thin undoped layer (also referred to as *channel*) located at the junction between two materials with different bandgaps. In this layer, high mobility is reached since the carriers are not subject to collisions with doping impurities and with the Si/SiO_2 lattice discontinuity like in conventional Si transistors. In addition, HEMTs enjoy outstanding properties like high breakdown field and high saturation drift velocity. All these benefits make such devices attractive for a large variety of high-frequency applications where high gain and low noise are required, like radars operating in extreme environments,

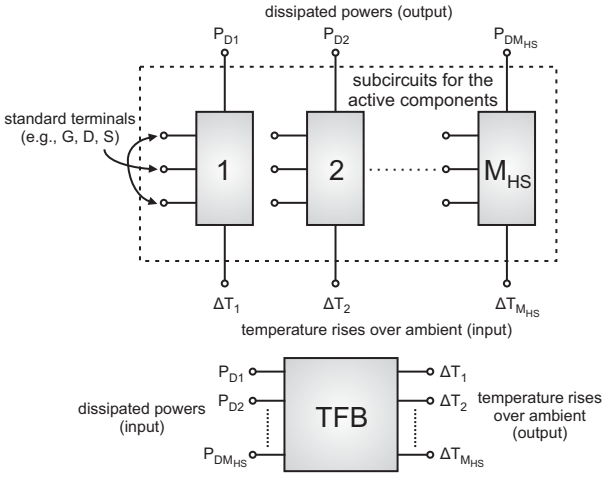

Fig. 3. Schematic representation of the strategy to perform an ET analysis in a circuit simulation tool.

microwave communications, and radio astronomy [27]. In particular, GaN HEMTs offer the highest output power and are considered the most appealing devices for microwave power amplifiers [28]–[32]. However, these transistors suffer from ET effects induced by the fast designer-induced growth in current (and power) density related to the higher signal bandwidth requirements for modern communications. The resulting raise in channel temperature reduces the low-field electron mobility, increases the source resistance, and lowers the saturation drift velocity, thereby entailing a distortion in the output characteristics, i.e., a decrease in the drain current for a given bias condition [33]–[37]. Such effects can be exacerbated in multifinger devices with an improperly-designed layout due to the thermal interactions between individual transistors.

Here we show that the approach presented in the previous Sections can be successfully used to perform a fast, yet accurate, dynamic ET analysis devised to improve the thermal ruggedness of multifinger and multicellular devices. In particular, we have examined the ET behavior of an 8-finger (i.e., 8-gate) AlGaN/GaN HEMT grown on a 70-μm-thick 6H-SiC layer [38] as a function of the key layout parameters, namely, finger width W and center-to-center spacing (also denoted as pitch) L_{GG} between fingers, as depicted in Fig. 4.

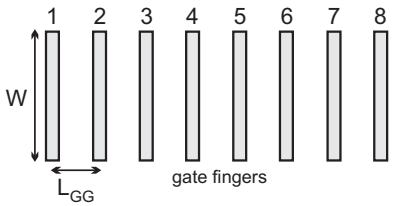

Fig. 4. Schematic top-view representation of the HEMT layout illustrating the gate fingers, the gate width W and pitch L_{GG}.

The device features a 0.4 μm gate length and a source-to-drain channel (i.e., the hetero-interface between the 25 nm-thick AlGaN and the 2 μm-thick GaN layers) amounting to 4 μm, and it was grown on a 7×5 mm^2 70-μm-thick 6H-SiC layer. The thermal conductivities of the main materials, namely, SiC, GaN and AlGaN were set to 370, 130 and 50 W/mK. Further details on the thermal, geometrical and technological parameters can be found in [37].

The required numerical simulations were supported by an *in-house* code that allows automatically drawing the 3-D transistor structure and building the mesh of the device within the environment of the commercial FEM software package Comsol [39]. In such thermal model each channel is associated to a thin heat source. In our analysis, W is varied in the range 75 μm to 150 μm, while L_{GG} spans from 15 μm to 45 μm.[1] It will be shown that W mainly influences the self-heating thermal impedances, whereas L_{GG} mainly impacts the mutual impedances between fingers. Fig. 5 illustrates a portion of the Comsol grid corresponding to the device under test for W=75 μm and L_{GG}=30 μm. The heat sources were placed in the portion of the channel corresponding to the projections of the gates. It can be inferred that the mesh was properly refined within the regions playing a major role from the thermal viewpoint thanks to the advanced features available in the latest Comsol releases. The number of elements (tetrahedra) is almost layout-independent, and amounts to about 2.5×10^5. The evaluation of the dynamic temperature field within the whole structure due to the activation of a single heat source required about 3 hours on a workstation equipped with 2 hexa-core Intel Xeon E7450 CPUs and 100 GB RAM. Exploiting the structure symmetry, only 4 transient simulations were needed to compute the thermal impedance matrix for a given layout configuration, which led to a total of about 12 hours. The dynamic estimation grid comprises the following 9 *estimation points*: (W, L_{GG})=(75, 15), (75, 30), (75, 45), (112.5, 15), (112.5, 30), (112.5, 45), (150, 15), (150, 30), (150, 45) μm. In order to improve the overall fitting accuracy, much less computationally-demanding steady-state thermal simulations were performed for 12 additional points: (W, L_{GG})=(75, 22.5) (75, 37.5), (93.75, 15), (93.75, 30), (93.75, 45), (112.5, 22.5), (112.5, 37.5), (131.25, 15), (131.25, 30), (131.25, 45), (150, 22.5), (150, 37.5) μm, only 20 minutes being required for each point. The 4 *validation points* needed to assess the model accuracy over design space points not used for its generation, are (W, L_{GG})=(93.75, 22.5), (93.75, 37.5), (131.25, 22.5), (131.25, 37.5) μm.

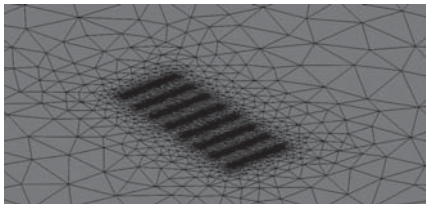

Fig. 5. Comsol mesh for the multi-gate HEMT under test with W=75 μm and L_{GG}=30 μm.

Once the parameterized macromodel has been extracted, the CPU time needed to perform a time-domain simulation of the thermal impedance matrix for assigned geometrical parameters is only 0.22 s on a normal PC equipped with an Intel Core2 Extreme CPU Q9300 2.53GHz and 8 GB RAM,

[1]It is worth noting that a variation in W modifies also the current handling capability of the whole device, which is instead independent of L_{GG}.

with a significant gain compared to the time/memory required by a conventional approach.

In order to fully characterize the accuracy of the proposed approach, the following errors were suitably defined:

- relative error exluding the thermal impedance for short times which is less relevant for ET simulations

$$Err_{rel}(\mathrm{Z_{ij}}) = \max_t \left[100 \cdot \left| \frac{\mathrm{Z_{ij}(t) - Z_{ij,model}(t)}}{\mathrm{Z_{ij}(t)}} \right| \right] \qquad (14)$$

$$\text{for } \mathrm{t} \geq \mathrm{t}^*, \mathrm{Z_{ij}}(\mathrm{t}^*) = 0.3\mathrm{R_{ij}}$$

- normalized relative error with respect to the steady-state values

$$Err_{norm}(\mathrm{Z_{ij}}) = \max_t \left[100 \cdot \left| \frac{\mathrm{Z_{ij}(t) - Z_{ij,model}(t)}}{\mathrm{Z_{ij}(t)}} \right| \right] \cdot \frac{\mathrm{R_{ij}}}{\mathrm{R_{max}}} \qquad (15)$$

$$\text{for } \mathrm{t} \geq \mathrm{t}^*, \mathrm{Z_{ij}}(\mathrm{t}^*) = 0.3\mathrm{R_{ij}}\,, \mathrm{R_{max}} = \max_{ij}(\mathrm{R_{ij}})$$

- steady-state relative and normalized relative errors: equations (15) and (14), respectively, for $t \to \infty$

Fig. 6 depicts the comparison between the FEM data and the macromodel output at the estimation points (a) for the self-heating term $Z_{11}(t)$ at L_{GG}=30 μm and W=75, 112.5, 150 μm, and (b) for the mutual impedances $Z_{12}(t)$ and $Z_{13}(t)$ at W=112.5 μm and L_{GG}=15, 30, 45 μm. Fig. 7 shows a similar comparison for the validation points, depicting (a) $Z_{11}(t)$ at L_{GG}=22.5 μm and W=93.75, 131.25 μm, and (b) $Z_{12}(t)$ and $Z_{13}(t)$ at W=131.25 μm and L_{GG}=22.5, 37.5 μm. In spite of the coarseness of the estimation grid, the macromodel exhibits a good agreement with the input data, and the maximum values of the previously defined errors at all validation points are reported in Table I. The corresponding errors at the estimation points assume lower values than in Table I, which is expected since the estimation points are used to generate the parameterized macromodel. Thanks to the additional steady-state estimation points, an overall accuracy improvement was achieved with respect to the authors' previous work [14]. The parameterized macromodel output is illustrated in Fig. 8, which shows the dependence of $Z_{11}(t)$ upon W for L_{GG}=30 μm, and of $Z_{12}(t)$ upon L_{GG} for W=112.5 μm.

The dynamic ET simulations of the device under test were performed through the popular tool PSPICE [40] by exploiting the strategy described in Section IV:

- each finger was described through a subcircuit implementing the model proposed in [41], which is conceived to ensure a good accuracy over a wide range of channel temperatures, if a proper parameter optimization is carried out;
- the TFB – generated for each layout configuration – was connected to the electrical schematic corresponding to the 8-finger device, each finger being represented by the aforementioned subcircuit. The number of RC cells for the equivalent Foster networks of the TBF was varying between 11 and 15 for the self-heating thermal impedances, while between 2 and 6 for the mutual thermal impedances.

TABLE I. PARAMETERIZED MACROMODEL VALIDATION ERRORS

Error definition	Value
Relative error (14)	10.8%
Normalized relative error (15)	2.75%
Steady-state relative error	10.4%
Steady-state normalied relative error	0.29%

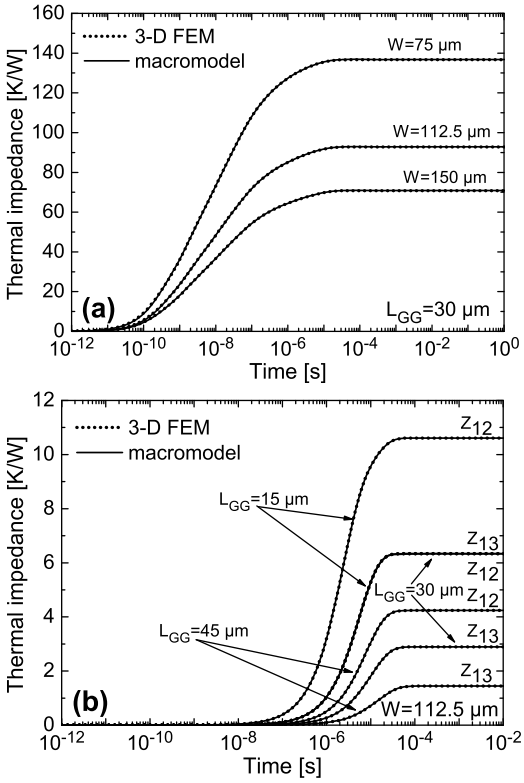

Fig. 6. Comparison between 3-D FEM (dotted lines) and macromodel results (solid) at the estimation points: (a) self-heating thermal impedance $Z_{11}(t)$ for transistors with L_{GG}=30 μm and W=75, 112.5, 150 μm; (b) mutual thermal impedances $Z_{12}(t)$ and $Z_{13}(t)$ for transistors with W=112.5 μm and L_{GG}=15, 30, 45 μm.

The device was biased by applying V_{GS}=0 V and a 200 kHz V_{DS}=30 V pulse train with a 20% duty cycle. Simulations were very fast (a CPU time amounting to a few seconds was needed to analyze the device behavior over a time range of hundreds of μs) and no convergence issues were encountered in spite of the sharp edges of the pulses. Fig. 9 reports the temperature rise of the hottest finger for various layout configurations by keeping constant (a) the gate width W, and (b) the pitch L_{GG}. Results can be summarized as follows. The temperature peak becomes lower with increasing L_{GG} (Fig. 9a) since the thermal coupling between gate fingers decreases. A less intuitive behavior is obtained by increasing W (Fig. 9b): the higher current handling capability due to the larger finger area is effectively counteracted by the reduction in self-heating thermal impedances, and only a marginal temperature growth is observed.

VI. CONCLUSIONS

This paper presents a parameterized macromodeling strategy conceived and developed for a fast prediction of the influence of design features on the dynamic electrothermal behavior of

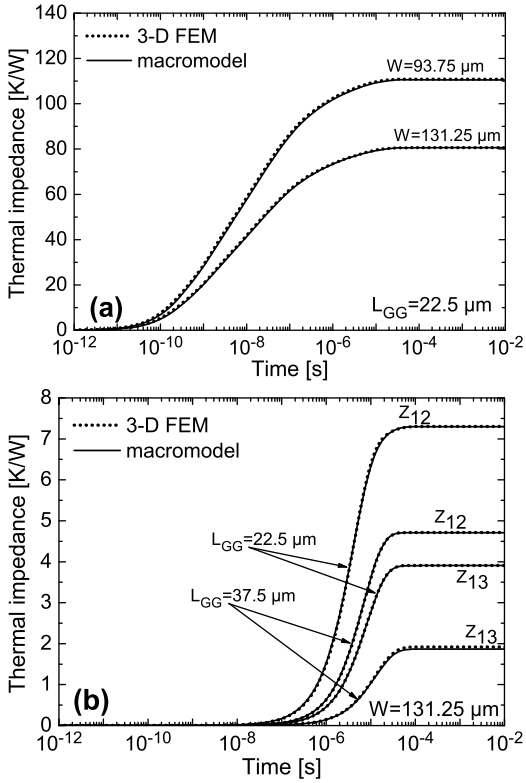

Fig. 7. Comparison between 3-D FEM (dotted lines) and macromodel results (solid) at the validation points: (a) self-heating thermal impedance $Z_{11}(t)$ for transistors with L_{GG}=22.5 μm and W=93.75, 131.25 μm; (b) mutual thermal impedances $Z_{12}(t)$ and $Z_{13}(t)$ for transistors with W=131.25 μm and L_{GG}=22.5, 37.5 μm.

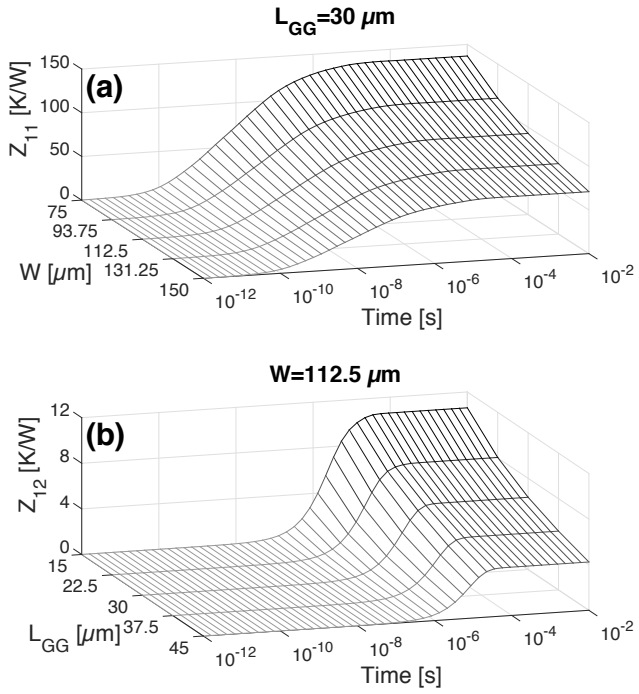

Fig. 8. Parameterized macromodel output for (a) self-heating thermal impedance $Z_{11}(t)$ as a function of time and W, and (b) mutual thermal impedance $Z_{12}(t)$ as a function of time and L_{GG}.

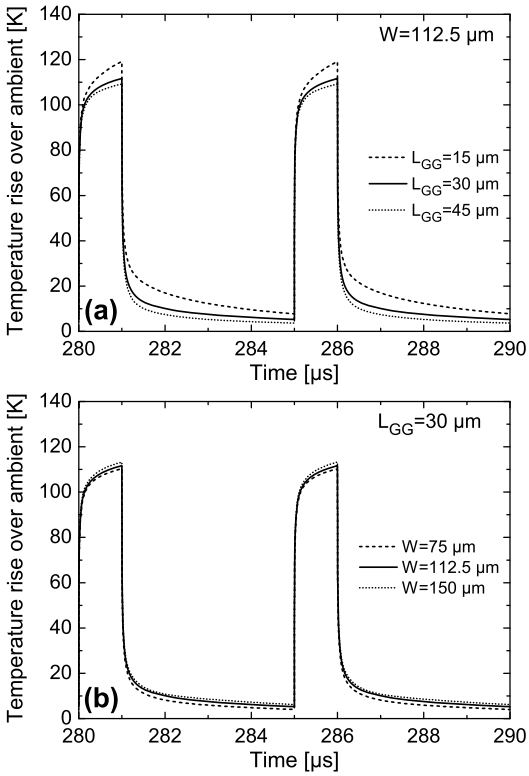

Fig. 9. ET simulation of a 8-finger HEMT biased with V_{GS}=0 V and a 200 kHz V_{DS}=30 V pulse train with a 20% duty cycle: temperature rise over ambient for the hottest finger at various layout configurations (a) at fixed W, and (b) at fixed L_{GG}.

electronic components and systems with multiple heat sources. A decomposition of the frequency-domain data samples of the thermal impedance helps to achieve a high model accuracy with a limited number of computationally expensive thermal simulations. The approach has been adopted to perform electrothermal simulations of an 8-finger AlGaN/GaN while taking into account the effects of key layout parameters, namely the gate width and gate-to-gate pitch, on the electrothermal behavior. The pre-processing 3-D FEM analysis has been carried out over an estimation grid including 9 points for dynamic and 12 points for steady-state simulations, respectively. It has been found that the resulting macromodel allows evaluating the transistor impedance matrix in much less than 1 s, while several hours are required when exploiting conventional FEM simulations. Moreover, a good accuracy was achieved over the 4 validation points, the normalized relative error being lower than 2.75%. This study witnesses that the proposed macromodeling strategy can successfully support the design workflow of electronic components and systems in order to face and solve various design tasks with great time saving.

ACKNOWLEDGMENT

This work was supported by the Research Foundation Flanders (FWO-Vlaanderen). Francesco Ferranti is a Post-Doctoral Research Fellow of FWO-Vlaanderen.

REFERENCES

[1] M. Pedram and S. Nazarian, "Thermal modeling, analysis, and management in VLSI circuits: Principles and methods," *Proc. IEEE*, vol. 94, no. 8, pp. 1487–1501, Aug. 2006.

[2] Y. Zhan, S. V. Kumar, and S. S. Sapatnekar, "Thermally-aware design," *Found. Trends Electron. Design Autom.*, vol. 2, no. 3, pp. 255–370, 2007.

[3] L. Codecasa, D. D'Amore, and P. Maffezzoni, "Compact modeling of electrical devices for electrothermal analysis," *IEEE Trans. Circuits Syst. I*, vol. 50, no. 4, pp. 465–476, Apr. 2003.

[4] L. Codecasa, "Compact models of dynamic thermal networks with many heat sources," *IEEE Trans. Compon. Packag. Technol.*, vol. 30, no. 4, pp. 653–659, Dec. 2007.

[5] D. Celo, X. Guo, P. Gunupudi, R. Khazaka, D. Walkey, T. Smy, and M. Nakhla, "The creation of compact thermal models of electronic components using model reduction," *IEEE Trans. Adv. Packag.*, vol. 28, no. 2, pp. 240–251, May 2005.

[6] V. d'Alessandro, M. de Magistris, A. Magnani, N. Rinaldi, and S. Russo, "Dynamic electrothermal macromodeling: an application to signal integrity analysis in highly integrated electronic systems," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 3, no. 7, pp. 1237–1243, Jul. 2013.

[7] V. d'Alessandro, A. Magnani, M. Riccio, Y. Iwahashi, G. Breglio, N. Rinaldi, and A. Irace, "Analysis of the UIS behavior of power devices by means of SPICE-based electrothermal simulations," *Microelectron. Reliab.*, vol. 53, no. 9, pp. 1713–1718, 2013.

[8] F. Ferranti, L. Knockaert, and T. Dhaene, "Guaranteed passive parameterized admittance-based macromodeling," *IEEE Trans. Adv. Packag.*, vol. 33, no. 3, pp. 623 –629, Aug. 2010.

[9] ——, "Parameterized S-parameter based macromodeling with guaranteed passivity," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 10, pp. 608–610, Oct. 2009.

[10] P. Triverio, M. Nakhla, and S. Grivet-Talocia, "Passive parametric macromodeling from sampled frequency data," in *Proc. IEEE Workshop on Signal Propagation on Interconnects (SPI)*, 2010, pp. 117–120.

[11] ——, "Passive parametric modeling of interconnects and packaging components from sampled impedance, admittance or scattering data," in *Proc. Electronic System-Integration Technology Conference (ESTC)*, 2010, pp. 1–6.

[12] F. Ferranti, L. Knockaert, and T. Dhaene, "Passivity-preserving parametric macromodeling by means of scaled and shifted state-space systems," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 10, pp. 2394–2403, Oct. 2011.

[13] F. Ferranti, T. Dhaene, and L. Knockaert, "Compact and passive parametric macromodeling using reference macromodels and positive interpolation operators," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 2, no. 12, pp. 2080–2088, Dec. 2012.

[14] F. Ferranti, T. Dhaene, S. Russo, A. Magnani, M. de Magistris, V. d'Alessandro, and N. Rinaldi, "Parameterized thermal macromodeling for fast and effective design of electronic components and systems," in *Proc. IEEE Workshop on Signal and Power Integrity (SPI)*, 2014.

[15] V. d'Alessandro, M. De Magistris, A. Magnani, N. Rinaldi, S. Grivet-Talocia, and S. Russo, "Time domain dynamic electrothermal macromodeling for thermally aware integrated system design," in *Proc. IEEE Workshop on Signal and Power Integrity (SPI)*, 2013, pp. 29–32.

[16] R. A. Horn and C. R. Johnson, *Topics in matrix analysis*. Cambridge University Press, 1994.

[17] V. Székely, "On the representation of infinite-length distributed RC one-ports," *IEEE Trans. Circuits Syst.*, vol. 38, no. 7, pp. 711–719, Jul. 1991.

[18] ——, "Identification of RC networks by deconvolution: chances and limits," *IEEE Trans. Circuits Syst.*, vol. 45, no. 3, pp. 244–258, Mar. 1998.

[19] B. Gustavsen and A. Semlyen, "Rational approximation of frequency domain responses by vector fitting," *IEEE Transactions on Power Apparatus and Systems*, vol. 14, no. 3, pp. 1052–1061, Jul. 1999.

[20] B. Gustavsen, "Improving the pole relocating properties of vector fitting," *IEEE Trans. Power Del.*, vol. 21, no. 3, pp. 1587–1592, Jul. 2006.

[21] M. de Magistris and M. Nicolazzo, "On the concretely passive realization of reduced circuit models based on convex constrained positive real fractions identification," in *Proc. IEEE Workshop on Signal and Power Integrity (SPI)*, 2011, pp. 29–32.

[22] U. Drofenik, D. Cottet, A. Musing, J.-M. Meyer, and J. W. Kolar, "Computationally efficient integration of complex thernal multi-chip power module models into circuit simulators," in *Proc. IEEE Power Conversion Conference*, 2007, pp. 550–557.

[23] W. B. Joyce, "Thermal resistance of heat sinks with temperature-dependent conductivity," *Solid-State Electronics*, vol. 18, no. 4, pp. 321 – 322, 1975.

[24] W. Batty and C. M. Snowden, "Electro-thermal device and circuit simulation with thermal nonlinearity due to temperature dependent diffusivity," *Electronics Letters*, vol. 36, no. 23, pp. 1966–1968, Nov 2000.

[25] F. Bonani and G. Ghione, "On the application of the Kirchhoff transformation to the steady-state thermal analysis of semiconductor devices with temperature-dependent and piecewise inhomogeneous thermal conductivity," *Solid-State Electronics*, vol. 38, no. 7, pp. 1409 – 1412, 1995.

[26] L. Codecasa, V. d'Alessandro, A. Magnani, and N. Rinaldi, "Compact dynamic modeling for fast simulation of nonlinear heat conduction in ultra-thin chip stacking technology," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 4, no. 11, pp. 1785–1795, Nov. 2014.

[27] L. F. Eastman and U. K. Mishra, "The toughest transistor yet," *IEEE Spectrum*, vol. 39, no. 5, pp. 28–33, May 2002.

[28] R. Schwindt, V. Kumar, O. Aktas, J.-W. Lee, and I. Adesida, "AlGaN/GaN HEMT-based fully monolithic X-band low noise amplifier," *Phys. Status Solidi*, vol. 2, no. 7, pp. 2631–2634, 2005.

[29] U. K. Mishra, L. Shen, T. E. Kazior, and Y.-F. Wu, "GaN-based RF power devices and amplifiers," *Proc. IEEE*, vol. 96, no. 2, pp. 287–305, Feb. 2008.

[30] K. W. Kobayashi, Y. Chen, I. Smorchkova, B. Heying, W.-B. Luo, W. Sutton, M. Wojtowicz, and A. Oki, "Multi-decade GaN HEMT cascode-distributed power amplifier with baseband performance," in *Proc. IEEE Radio Frequency Integrated Circuits Symposium (RFICS)*, 2009, pp. 369–372.

[31] K. Krishnamurthy, J. Martin, D. Aichele, and D. Runton, "A decade bandwidth 90 W GaN HEMT push-pull power amplifier for VHF/UHF applications," in *Proc. IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, 2011.

[32] F. Yamaki, K. Inoue, N. Ui, A. Kawano, and S. Sano, "A 65% drain efficiency GaN HEMT with 200 W peak power for 20 V to 65 V envelope tracking base station amplifier," in *Proc. IEEE International Microwave Symposium Digest*, 2011.

[33] R. Gaska, A. Osinsky, J. Yang, and M. S. Shur, "Self-heating in high-power AlGaN-GaN HFETs," *IEEE Electron Device Lett.*, vol. 19, no. 3, pp. 89–91, Mar. 1998.

[34] J. Albrecht, R. Wang, P. Ruden, M. Farahmand, and K. Brennan, "Electron transport characteristics of GaN for high temperature device modeling," *J. Appl. Phys*, vol. 83, no. 9, pp. 4777–4781, May 1998.

[35] W.-C. Liu, K.-H. Yu, R.-C. Liu, K.-W. Lin, K.-P. Lin, C.-H. Yen, C.-C. Cheng, and K.-B. Thei, "Investigation of temperature-dependent characteristics of an n^+/-InGaAs/n-GaAs composite doped channel HFET," *IEEE Trans. Electron Devices*, vol. 48, no. 12, pp. 2677–2683, Dec. 2001.

[36] J. Kuzmík, P. Javorka, A. Alam, M. Marso, M. Heuken, and P. Kordoš, "Determination of channel temperature in AlGaN/GaN HEMTs grown on sapphire and silicon substrates using DC characterization method," *IEEE Trans. Electron Devices*, vol. 49, no. 8, pp. 1496–1498, Aug. 2002.

[37] S. Russo, V. d'Alessandro, M. Costagliola, G. Sasso, and N. Rinaldi,

"Analysis of the thermal behavior of AlGaN/GaN HEMTs," *Mater. Sci. Eng. B–Adv.*, vol. 177, no. 15, pp. 1343–1351, 2012.

[38] M. Peroni, P. Romanini, A. Pantellini, L. Mariucci, A. Minotti, G. Ghione, V. Camarchia, E. Limiti, A. Serino, and A. Chini, "Design, fabrication, and characterization of Γ-gate GaN HEMT for high-frequency/wide-band applications," in *Proc. Workshop On Compound Semiconductor Devices and Integrated Circuits held in Europe*, 2007, pp. 371–378.

[39] Comsol Multiphysics 3.5a, *User's Manual*, COMSOL AB, Stockholm, Sweden, 2008.

[40] PSPICE 16.5, *User's Manual*, Cadence OrCAD, 2011.

[41] F. Bertoluzza, G. Sozzi, N. Delmonte, and R. Menozzi, "Hybrid large-signal/lumped-element electro-thermal modeling of GaN-HEMTs," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 12, pp. 3163–3170, Dec. 2009.

Francesco Ferranti (M'10) received the Ph.D. degree in electrical engineering from Ghent University, Ghent, Belgium, in 2011. He is currently a Post-Doctoral Research Fellow of the Research Foundation Flanders (FWO-Vlaanderen) at the Department of Fundamental Electricity and Instrumentation, Vrije Universiteit Brussel, Brussels, Belgium. His current research interests include parameterized macromodeling, parameterized model order reduction, system identification, signal integrity, electromagnetic compatibility and uncertainty quantification.

Alessandro Magnani received the M.Sc. degree in electronics engineering (*summa cum laude*) from the University Federico II, Naples, Italy, in 2011. He is currently a Ph.D. student with the Department of Electrical Engineering and Information Technology of the same University. His present research interests include the thermal and electrothermal modeling of semiconductor devices and circuits, with emphasis on the extraction of compact models.

Vincenzo d'Alessandro is an Associate Professor at the Department of Electrical Engineering and Information Technology of University Federico II, Naples, Italy, where he teaches semiconductor devices and digital circuits. His current research interests include thermal modeling and electrothermal simulation of semiconductor devices, circuits, and systems, with particular emphasis on bipolar technology, and modeling/simulation of photovoltaic plants. He has coauthored over 120 papers in refereed international journals and conference proceedings, as well as a book, two book chapters and one patent. He is a reviewer for IEEE TRANSACTIONS ON ELECTRON DEVICES, IEEE ELECTRON DEVICE LETTERS, IEEE JOURNAL OF PHOTOVOLTAICS, *Solid-State Electronics*, *Microelectronics Reliability*, *International Journal of Numerical Modeling*, as well as for international conferences.

Salvatore Russo received the Laurea degree in electronics engineering and the Ph.D. degree with the dissertation "Measurement and simulation of electrothermal effects in solid-state devices for RF applications" from the University Federico II, Naples, Italy, in 2007 and 2010, respectively. He was a Visiting Scientist with the ECTM, Delft, The Netherlands, in 2008, where he worked on the simulation and modeling of electrothermal effects in last-generation silicon-on-glass RF transistors. His current research interests include electrothermal and thermal modeling/simulation of semiconductor devices, with particular regard to HBTs, BJTs, and HEMTs.

Niccolò Rinaldi (M'95) is a Full Professor at the Department of Electrical Engineering and Information Technology of University Federico II, Naples, Italy. He is currently member of the Executive Committee of the IEEE Bipolar/BiCMOS Circuits and Technology Meeting, and vice-chairman of the IEEE Electron Device Chapter (Central & South Italy Section). He has authored or coauthored over 130 publications in international journals and conferences. Prof. Rinaldi is a reviewer for IEEE TRANSACTIONS ON ELECTRON DEVICES, IEEE ELECTRON DEVICE LETTERS, *Solid-State Electronics*, *Microelectronics Journal*, *Fizika A&B*, *International Journal of Electronics*, as well as for international conferences.

Tom Dhaene (SM'05) received the Ph.D. degree in Electrotechnical Engineering from the University of Ghent, Ghent, Belgium, in 1993. In 1993, he joined the EDA company Alphabit (now part of Agilent). He was one of the key developers of the planar EM simulator ADS Momentum. Since September 2000, he has been a Professor with the Department of Mathematics and Computer Science, University of Antwerp, Antwerp, Belgium. Since October 2007, he has been a Full Professor with the Department of Information Technology (INTEC), Ghent University, Ghent. He has authored or coauthored more than 250 peer-reviewed papers and abstracts in international conference proceedings, journals and books about computational science and engineering, numerical analysis, and computer science. He has holds five U.S. patents.

Massimiliano de Magistris (M'94, SM'12) is an Associate Professor at the Department of Electrical Engineering and Information Technology of University Federico II, Naples, Italy. His main research interests have been in the areas of plasmas and accelerators engineering and applied electromagnetics. Currently he is addressing the macro modeling of electrical and electronic systems, as well as complex networks analysis. He has been author or co-author of more than 70 peer reviewed scientific papers for international journals and conferences, and is a reviewer for several IEEE journals.